Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (currently amended) A subcode-data generating circuit, which generates subcode data including subcode component data which indicates ~~at least one of~~ time information and additional subcode component data which indicates information other than the time information, said circuit comprising:

a first generating portion for automatically generating the subcode component data which indicates the time information;

a second generating portion for automatically generating the additional subcode component data which indicates the information other than the time information; and

a selecting portion which selects an output of at least one of said first and second generating portions,

wherein said first and second generating portions operate according to first and second commands, respectively.

2. (original) The subcode-data generating circuit, as claimed in claim 1, wherein said second generating portion comprises a plurality of generating portions provided separately.

3. (currently amended) A subcode-data generating circuit, which generates subcode data including subcode component data which indicates ~~at least one of~~ time information and additional subcode component data which indicates information other than the time information, said

circuit comprising:

a first generating portion for automatically generating the subcode component data which indicates the time information;

a second generating portion for automatically generating the additional subcode component data which indicates the information other than the time information;

a selecting portion which selects an output of at least one of said first and second generating portions; and

a memory ~~in which commands for automatic generation of the subcode component data are written~~, wherein ~~the commands include~~ first commands for automatic generation of the subcode component data which indicates the time information, which first commands are written collectively in a first area of said memory, and second commands for automatic generation of the additional subcode component data which indicates the information other than the time information, which second commands are written collectively in a second area of said memory, are written.

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4. (previously presented) The subcode-data generating circuit, as claimed in claim 3, wherein:

said second generating portion comprises a plurality of generating portions provided separately;

said second area of said memory comprises a plurality of areas corresponding to said plurality of generating portions; and

commands of the second commands are written collectively in each area of said plurality of areas, which commands correspond to a respective one of said plurality of generating portions.

5. (previously presented) A subcode-data generating circuit, which generates and selects subcode data including subcode component data, a state of said subcode component data alternating between a high state and a low state at a predetermined period, said circuit comprising:

a toggle generating portion which independently generates subcode component data, the state of said subcode component data alternating between the high state and the low state at the predetermined period; and

B1 a selecting portion which selects one of the subcode component data of said toggle generating portion,

wherein the state of said subcode component data ~~alternating~~ alternates between the high state and the low state at the predetermined period, the alternating period being based on a number of data sectors ~~relating~~ corresponding to ~~pre-alternating data of~~ the subcode component data prior to the alternation.